CLAIMS

What is claimed is:

1. A method of forming a contact in a flash memory device that improves the depth of focus (DOF) margin and the overlay margin between a plurality of stacked gate layers and the respective contact, comprising the steps of:

forming a plurality of stacked gate layers on a semiconductor substrate, wherein each stacked gate layer extends in a predefined direction and is substantially parallel to other stacked gate layers;

depositing an interlayer insulating layer over the plurality of stacked gate layers;

patterning a contact hole between a first stacked gate layer of the plurality of stacked gate layers and a second stacked gate layer of the plurality of stacked gate layers, wherein the contact hole is an elongated shape; and

depositing a conductive layer in the contact hole.

2. The method of claim 1, wherein the step of patterning a contact hole between a first stacked gate layer and a second stacked gate layer includes aligning a major axis of the contact hole substantially parallel to the predefined direction of the stacked gate layers.

3. The method of claim 1, wherein the step of patterning a contact hole between a first stacked gate layer and a second stacked gate layer includes aligning a minor axis of the contact hole substantially perpendicular to the predefined direction of the stacked gate layers.

4. The method of claim 1, further comprising the step of:

removing a portion of the conductive layer that is outside the contact hole to leave the conductive layer in the contact hole.

5. The method of claim 1, wherein the step of patterning a contact hole between a first stacked gate layer and a second stacked gate layer includes forming a minor axis of the contact hole to be about 71 percent to about 90 percent of a major axis of the contact hole.

6. The method of claim 1, wherein the step of patterning a contact hole in an elongated shape includes patterning the contact hole in the shape of an ellipse.

7. The method of claim 1, wherein the step of patterning a contact hole in an elongated shape includes patterning the contact hole in the shape of a rectangle.

8. A flash memory device, comprising:

a plurality of stacked gate layers, wherein each stacked gate layer extends in a predefined direction and is substantially parallel to other stacked gate layers; and

a contact formed between a first stacked gate layer of the plurality of stacked gate layers and a second stacked gate layer of the plurality of stacked gate layers, wherein the contact is formed in an elongated shape.

9. The flash memory device of claim 8, wherein the contact includes a major axis, and the major axis is substantially parallel to the predefined direction of the stacked gate layers.

10. The flash memory device of claim 8, wherein the contact includes a minor axis, and the minor axis is substantially perpendicular to the predefined direction of the stacked gate layers.

11. The flash memory device of claim 8, wherein the contact is a V_{SS} contact.

12. The flash memory device claim 8, wherein a minor axis of the contact is about 71 percent to about 90 percent of a major axis of the contact.

13. The flash memory device of claim 8, wherein the contact hole is in the shape of an ellipse.

14. The flash memory device of claim 8, wherein the contact hole is in the shape of a rectangle.